What is claimed is:

1. A semiconductor device comprising:

an insulating film formed over a semiconductor substrate; and

a capacitor having a lower electrode, a dielectric film, and an upper electrode, that are formed on the insulating film;

wherein side walls of the lower electrode, the dielectric film, and the upper electrode form one surface, and

a thickness of the upper electrode in both sides is formed thinner than that in a center.

2. A semiconductor device according to claim 1, wherein the lower electrode is formed like a stripe shape, and

a planar shape of the dielectric film is formed similarly to a planar shape of the upper electrode.

3. A semiconductor device according to claim 1, wherein the upper layer portion is formed into a rectangular shape.

4. A semiconductor device according to claim 1, wherein the lower electrode and the dielectric film are formed like a stripe shape respectively, and

the upper electrode is formed in plural on the dielectric film.

5. A semiconductor device according to claim 4, wherein widths of the dielectric film and the lower

electrode are narrowed between the upper electrodes.

6. A semiconductor device according to claim 1, wherein a thickness of the upper electrode on its side portion is more than 20 nm.

7. A semiconductor device comprising:

an insulating film formed over a semiconductor substrate; and

a capacitor having a lower electrode, a dielectric film, and an upper electrode, that are formed on the insulating film;

wherein side walls of the lower electrode, the dielectric film, and the upper electrode form one surface, and

the upper electrode has a lower layer and an upper layer that are formed of different materials, and the upper layer is formed of material that has a smaller etching rate than the lower layer under conditions that the lower electrode or the dielectric film is etched.

8. A semiconductor device according to claim 7, wherein the lower electrode is formed like a stripe shape, and

a planar shape of the dielectric film is formed similarly to a planar shape of the upper electrode.

9. A semiconductor device according to claim 7, wherein the upper layer portion is formed into a rectangular shape.

10. A semiconductor device according to claim 7,

wherein the lower electrode and the dielectric film are formed like a stripe shape respectively, and

the upper electrode is formed in plural on the dielectric film.

11. A semiconductor device according to claim 7, wherein widths of the dielectric film and the lower electrode are narrowed between the upper electrodes.

12. A semiconductor device according to claim 7, wherein a thickness of the upper electrode on its side portion is more than 20 nm.

13. A manufacturing method of a semiconductor device comprising the steps of:

forming sequentially a first conductive film, a dielectric film, and a second conductive film, that constitute a capacitor, on an insulating film formed over a semiconductor substrate;

forming a first resist pattern on the second conductive film;

forming an upper electrode of the capacitor by etching the second conductive film while using the first resist pattern as a mask;

removing the first resist pattern;

forming a second resist pattern, that have a width equal to or smaller than a pattern width of the upper electrode of the capacitor, on the upper electrode of the capacitor; and

etching at least one of the dielectric film and the

first conductive film by using the second resist pattern as a mask, while exposing a part of an upper surface of the upper electrode of the capacitor by retreating side portion of the second resist pattern.

14. A manufacturing method of a semiconductor device according to claim 13, further comprising the steps of:

forming the upper electrode in plural at a distance in one direction;

forming the second resist pattern into stripe shapes to pass over the upper electrodes;

forming a stripe-like dielectric film of the capacitor under the upper electrodes by etching the dielectric film while using the second resist pattern as a mask; and

forming a stripe-like lower electrode of the capacitor under the stripe-like dielectric film by etching the first conductive film while using the second resist pattern as a mask.

15. A manufacturing method of a semiconductor device according to claim 14, wherein the stripe-like dielectric film and the stripe-like lower electrode are formed narrow between the upper electrodes.

16. A manufacturing method of a semiconductor device according to claim 13, further comprising the steps of:

patterning the dielectric film for the capacitor by

etching while using the second resist pattern as a mask, and then removing the second resist pattern;

forming a third resist pattern, that has a width equal to or smaller than a pattern width of the upper electrode of the capacitor, on the upper electrode of the capacitor and the dielectric film of the capacitor; and

forming the lower electrode of the capacitor by etching the first conductive film while using the third resist pattern as a mask, while exposing a part of an upper surface of the upper electrode of the capacitor by retreating side portion of the third resist pattern.

17. A manufacturing method of a semiconductor device according to claim 13, further comprising the steps of:

patterning the dielectric film having a planar shape, that is similar to a planar shape of the upper electrode of the capacitor, by etching the dielectric film while using the first resist pattern as a mask after the upper electrodes of the capacitor are formed; and

forming the lower electrode of the capacitor by etching the first conductive film while using the second resist patterns as a mask.

18. A manufacturing method of a semiconductor device according to claim 13, wherein adhesion of conductive etching product onto side wall of the upper electrode of the capacitor and the lower electrode of the capacitor is prevented during etching of the dielectric

film or the first conductive film by adjusting a chlorine ratio, a total gas flow rate, a bias power, or a degree of vacuum while using a plasma containing chlorine and argon to control a retreating speed of the resist pattern.

19. A manufacturing method of a semiconductor device according to claim 13, wherein respective thicknesses of the first conductive film, the dielectric film, and the second conductive film are set such that an original width of the upper electrode of the capacitor is assured at a time when the etching of the dielectric film and the first conductive film is finished.

20. A manufacturing method of a semiconductor device according to claim 13, wherein side portions of the upper electrode of the capacitor are retreated during the etching of the dielectric film or the first conductive film, and an amount of retreat is set to exceed an amount of displacement of the upper electrode of the capacitor from the pattern when the second resist patterns or the third resist pattern is formed.

21. A manufacturing method of a semiconductor device according to claim 13, wherein side portions of the upper electrode of the capacitor are retreated during the etching of the dielectric film or the first conductive film, and an amount of retreat is set to exceed a width that is required to remove corner portions of the pattern of the upper electrode of the capacitor.

22. A manufacturing method of a semiconductor

device according to claim 13, further comprising the step of:

forming an etching preventing film, that prevents the etching of the upper electrode of the capacitor during the etching of the dielectric film or the first conductive film, on the upper electrode of the capacitor.

23. A manufacturing method of a semiconductor device according to claim 22, wherein the etching preventing film is formed of strontium ruthenium oxide.